CLAIMS

What is claimed is:

1. A method, comprising:

providing a substrate having a plurality of features comprising a first material;

forming a layer over the substrate and the plurality of features, the layer comprising a second material;

removing the layer down to upper surfaces of the plurality of features, thereby exposing the plurality of features; and

removing the plurality of features.

2. The method as set forth in claim 1, wherein:

the removing of the plurality of features leaves behind portions of the layer; and

a pitch of adjacent features of the plurality of features, measured before the plurality of features is removed, is greater than a pitch of adjacent portions of the layer.

3. The method as set forth in claim 1, wherein:

the second material comprises polysilicon; and

the removing of the layer down to upper surfaces of the plurality of features forms a plurality of gates.

4. The method as set forth in claim 1, wherein:

the providing of a substrate includes providing a substrate having a first dielectric disposed thereon, the first dielectric being disposed between the substrate and the plurality of features; and

the forming of a layer over the substrate includes forming a second dielectric on the substrate and forming the layer on the second dielectric, so that the second dielectric is disposed between the substrate and the layer.

5. The method as set forth in claim 1, wherein:

the providing of a substrate includes providing a substrate having a first dielectric disposed thereon and removing the first dielectric from areas not covered by the features; and

the forming of a layer over the substrate includes forming a second dielectric on the areas and forming the layer on both the second dielectric and the features, so that the second dielectric is disposed between the substrate and the layer.

6. The method as set forth in claim 2, wherein:

the first and second dielectrics comprise silicon dioxide; and

prior to the forming of a layer over the substrate, the first dielectric is removed from areas of the substrate not covered by the plurality of features and the second dielectric is deposited onto the areas.

7. The method as set forth in claim 3, wherein:

the removing of the plurality of features leaves behind portions of the layer; and

a pitch of adjacent features of the plurality of features, measured before the plurality of features is removed, is greater than a pitch of adjacent portions of the layer.

8. The method as set forth in claim 4, wherein:

the second material comprises polysilicon; and

the removing of the layer down to upper surfaces of the plurality of features forms a plurality of gates.

9. The method as set forth in claim 5, wherein:

the providing of a substrate having a plurality of features is preceded by using a photolithography process to form the plurality of features on the substrate; and

a pitch of adjacent features of the plurality of features is as small as the photolithography process will allow.

10. A structure formed using the method of claim 1.

11. A structure formed using the method of claim 2.

12. A structure formed using the method of claim 6.

13. A method for forming a semiconductor device having a reduced pitch, comprising:

providing a substrate having a first insulating layer formed thereon;
forming a material layer on the first insulating layer;
forming a photoresist layer on the material layer;
etching the material layer using the photoresist layer as an etch mask;
removing the photoresist layer;
removing an exposed portion of the first insulating layer;
forming a second insulating layer on an exposed portion of the substrate;
depositing a conductive layer over the material layer and second insulating layer;
etching back the conductive layer to expose the material layer; and
removing the material layer.

14. The method as set forth in claim 13, wherein:
the first insulating layer is a pad oxide;
the material layer comprises silicon nitride;
the second insulating layer is a gate oxide;
the conductive layer comprises polysilicon.

15. The method as set forth in claim 14, wherein:
the photoresist layer is a trimmed photoresist layer; and
the etching of the conductive layer forms a plurality of gates.

16. The method of claim 15, wherein:
the pad oxide layer is formed using a thermal process;

the forming of the silicon nitride layer on the pad oxide layer comprises using a chemical vapor deposition process; and

the forming of the trimmed photoresist layer on the silicon nitride layer comprises forming a patterned photoresist layer on the silicon nitride layer and etching the patterned photoresist layer.

17. The method of claim 16, wherein:

the etching of the patterned photoresist layer comprises etching the patterned photoresist layer at an etch rate that is greater than an etch rate at which the silicon nitride layer is etched;

the etching of the patterned photoresist layer is terminated before a substantial portion of the silicon nitride layer is removed; and

the etching of the silicon nitride layer comprises etching the silicon nitride layer at an etch rate that is greater than an etch rate at which the pad oxide is etched.

18. The method of claim 15, wherein:

the removing the trimmed photoresist layer comprises using a dry stripping process or a wet stripping process; and

the removing of the exposed portion of the pad oxide layer comprises using a wet etching process.

19. The method of claim 15, wherein an amount of the conductive layer deposited on the gate oxide layer is determined by an expected thickness of the plurality of gates.

20. A structure formed using the method of claim 13.

21. A structure formed using the method of claim 15.

22. A structure comprising:

a plurality of gate conductors laterally spaced apart on a substrate;

a plurality of first dielectric portions laterally spaced apart on the substrate, wherein first dielectric portions are laterally interspersed between gate conductors; and

a plurality of second dielectric portions, each of the second dielectric portions being disposed between the substrate and one of the gate conductors.

23. The structure as set forth in claim 22, wherein a pitch of the gate conductors is less than pitch that a photolithography process will allow.

24. The structure as set forth in claim 22, wherein a thickness of the first dielectric is different than a thickness of the second dielectric.

25. The structure as set forth in claim 22, wherein the first dielectric is a pad oxide and the second dielectric is a gate oxide.

26. The structure as set forth in claim 25, wherein the pad oxide is thicker than the gate oxide.